```
┌─────────────────────────────┐
│         Wafer Sort          │
│ (Datalog repair solutions for│  ~ 10
│  all repairable devices using│
│      BISR Flarescan mode)   │
└─────────────────────────────┘
               │
               ▼
┌─────────────────────────────┐
│ Post-process repair solutions to│
│ determine which fuses need to│  ~ 12
│ be blown (compute amount of │
│     repair on each device)  │
└─────────────────────────────┘
               │
               ▼
┌─────────────────────────────┐
│   Burn the fuses to program │  ~ 14
│  repair solution on the device│
└─────────────────────────────┘
               │
               ▼
┌─────────────────────────────┐
│ Use the power-on state machine to│
│ load fuse values into the memories│  ~ 16
│      using the fusescan mode│
└─────────────────────────────┘
```
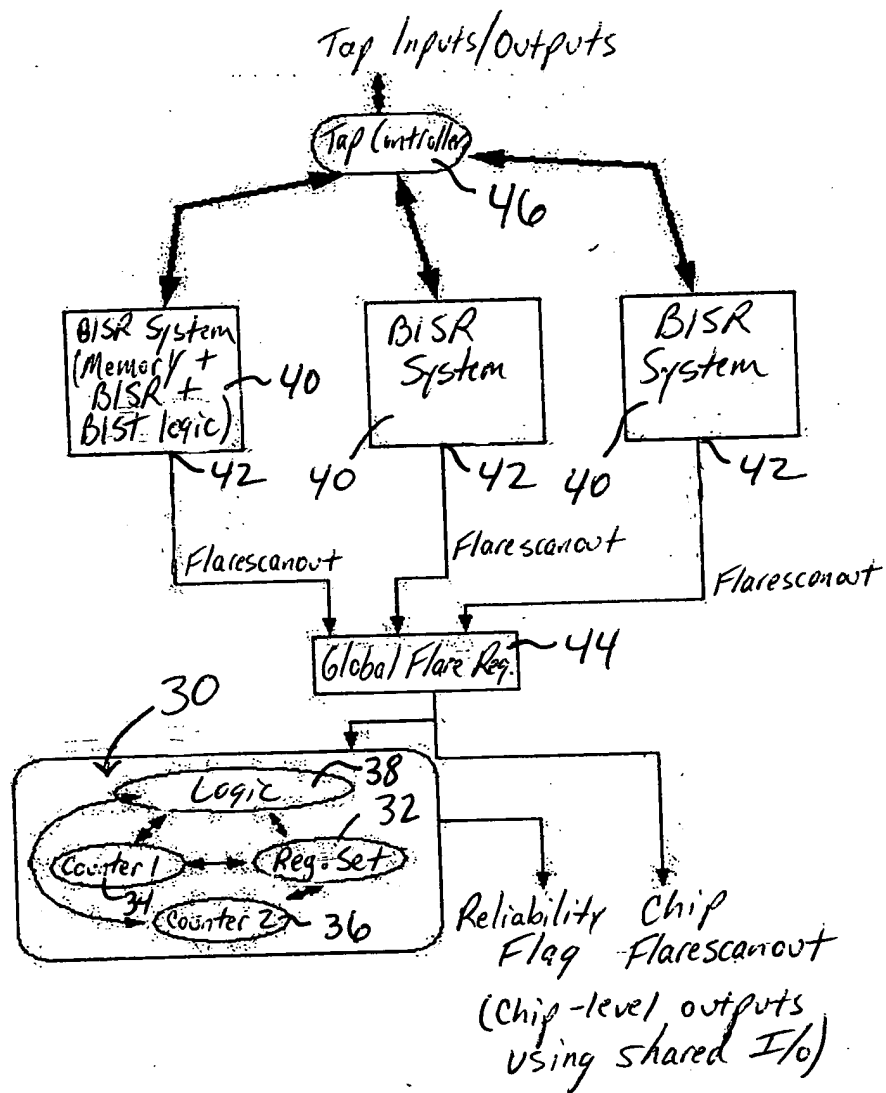
Prior Art

Figure 1

Run mode configured to make
an on-chip assessment of amount
of repaired memories and flag any
device failed when it exceeds a certain limit
– build a counter as part of BISR which
is thereafter loaded through a test pattern
during production testing that establishes
the threshold for pass/fail criteria

~ 20

Run power-on state machine configured
to load a computed repair solution and
thereafter test the memories for any additional
failures and, if there are any, repair them
(provided enough redundant elements are available)

~ 22

Figure 2

Tap Inputs/Outputs

Tap Controller ~46

BISR System
(Memory +
BISR +
BIST logic) ~40

~42

Flarescanout

BISR
System

40

~42 40

Flarescanout

BISR
System

~42

Flarescanout

Global Flare Reg. ~44

30

Logic ~38

32

Counter 1 ← → Reg. Set

34

Counter 2 ~36

Reliability   Chip
Flag   Flarescanout

(Chip-level outputs
using shared I/o)

Figure 3